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AMENDMENT TRANSMITTAL LETTERDocket No.
FIS920030199US1Application No.
10/604,607Filing Date
August 4, 2003Examiner
Thanh T. NguyenArt Unit
2813Applicant(s): **Huajie Chen et al.**Invention: **STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SEMICONDUCTOR REGIONS UNDERLYING SOURCE AND DRAIN REGIONS (As Amended)****TO THE COMMISSIONER FOR PATENTS**

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

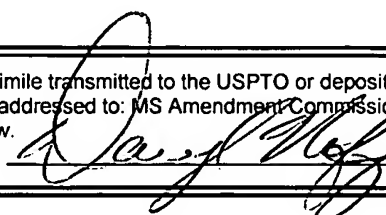
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	31	32	0		
Independent Claims	3	- 3	0		
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					

☒ Large Entity☐ Small Entity☒ No additional fee is required for this amendment.☐ Please charge Deposit Account No. _____ in the amount of \$ _____.
A duplicate copy of this sheet is enclosed.☐ A check in the amount of \$ _____ to cover the filing fee is enclosed.☐ Payment by credit card. Form PTO-2038 is attached.☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0458** as described below. A duplicate copy of this sheet is enclosed.☒ Credit any overpayment.☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Daryl K. Neff

Attorney Reg. No.: **38,253**Dated: **October 18, 2004**

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: MS Amendment Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: October 18, 2004 Signature:  (Daryl K. Neff)



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MS Amendment, Commissioner for Patents, Alexandria, VA 22313-1450 on this date: October 18, 2004

Name of Depositor:

Daryl K. Neff

Signature & Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Huajie Chen, et al.	Date: October 18, 2004
Serial Number: 10/604,607	Examiner: Thanh T. Nguyen
Filed: August 4, 2003	Group Art Unit: 2813
Title: STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SEMICONDUCTOR REGIONS UNDERLYING SOURCE AND DRAIN REGIONS (As Amended)	H. Daniel Schnurmann IBM Corporation D/18G, B/300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

AMENDMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated July 16, 2004, Applicants submit the following amendments and remarks for the Examiner's consideration.

Title of Invention:

Please amend the title to read:

STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS
TRANSISTORS HAVING LATTICE-MISMATCHED SEMICONDUCTOR REGIONS
UNDERLYING SOURCE AND DRAIN REGIONS